REMARKS

The final Office Action rejects claims 14, 15, 25, 26, and 32 under 35 U.S.C. § 103(a) as unpatentable over YOKOYAMA et al. (U.S. Patent No. 5,303,344) in view of ALBAL et al. (U.S. Patent No. 4,821,265), and further in view of STONER et al. (U.S. Patent No. 6,052,383); and allows claims 16-24, 27-31, 33, and 34. Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection.

By the present amendment, Applicants propose amending claims 19 and 24 to improve form. No new matter has been added by way of the present amendment. Claims 14-34 remain pending.

Applicants note with appreciation the indication that claims 16-24, 27-31, 33, and 34 are allowable over the art of record.

Claims 14, 15, 25, 26, and 32 stand rejected under 35 U.S.C. § 103(a) as unpatentable over YOKOYAMA et al. in view of ALBAL et al., and further in view of STONER et al. Applicants respectfully traverse this rejection.

Independent claim 14 is directed to a packet processing apparatus for converting packet data through a plurality of layers. The apparatus includes a packet memory for storing at least a user information portion of the packet data; and a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission, wherein the lower layer processing portion reads the header portion from the shared memory. The lower layer

processing portion and the higher layer processing portion access a same memory space of the shared memory through physically different memory buses. YOKOYAMA et al., ALBAL et al., and STONER et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, YOKOYAMA et al., ALBAL et al., and STONER et al. do not disclose or suggest a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission. The Examiner relies on col. 9, lines 16-20, 30-35, and 59-62, of YOKOYAMA et al. for allegedly disclosing these features (final Office Action, pg. 2). Applicants respectfully disagree.

> At col. 9, lines 16-20, YOKOYAMA et al. discloses:
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> The data transfer processor unit 100-3 of the data link layer first generates the LLC header in accordance with the contents of the third entry E3 of the command descriptor 31 read from the buffer memory as in the network layer (steps 1014 and 1015).

This section of YOKOYAMA et al. discloses that a data transfer processor 100-3 of a data link layer generates a logical link control (LLC) header in accordance with a portion of a command descriptor read from a buffer. This section of YOKOYAMA et al. in no way discloses or suggests a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer

processing operations, and read by the lower layer processing portion at a time of the packet data transmission, as recited in claim 14.

At col. 9, lines 26-35, YOKOYAMA et al. discloses:

> The MAC control processor 50 which has received the CDCI actuates the MAC LSI 40 in accordance with the command read from the fourth entry E4 of the command descriptor 31, whereby data including a header H2 to H4 is read from the buffer memory 30, and added to header H1, H1' to form a communication header which is then supplied to the network 3.
>
> The data receiving operation of the protocol processor 10 will be described with reference to FIGS. 13, 14 and 15.

This section of YOKOYAMA et al. discloses that a header H2 to H4 is read from a buffer and added to header H1, H1' to form a communication header, which is then supplied to a network 3. This section of YOKOYAMA et al. in no way discloses or suggests a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission, as recited in claim 14. Instead, this section of YOKOYAMA et al. merely discloses supplying headers to a network 3.

At col. 9, lines 59-66, YOKOYAMA et al. discloses:

> If the LLC header is the UI frame, and if the UI frame is normal, the data transfer processor unit 100-3 generates the primitive to the network layer in the third entry E3 of the command descriptor 31 (step 1034), and supplies the CDID previously received from the primitive path 22-4 to the primitive path 22-3, thereby starting the data transfer processor unit 100-2 of the network layer (step 1035).

This section of YOKOYAMA et al. discloses that data transfer processor unit 100-3 provides an address (CDID) to a primitive path 22-3 to start data transfer processor unit 100-2 of the network layer. This section of YOKOYAMA et al. in no way discloses or suggests a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission, as recited in claim 14.

If this rejection is maintained, Applicants respectfully request the Examiner to explain how the above sections of YOKOYAMA et al. can reasonably be construed to disclose a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission, as recited in claim 14.

The disclosures of ALBAL et al. and STONER et al. do not remedy the above deficiencies in the disclosure of YOKOYAMA et al.

For at least the foregoing reasons, Applicants submit that claim 14 is patentable over YOKOYAMA et al., ALBAL et al., and STONER et al., whether taken alone or in any reasonable combination.

Independent claims 15, 25, and 26 recite features similar to features described above with respect to claim 14. Therefore, claims 15, 25, and 26 are patentable over

YOKOYAMA et al., ALBAL et al., and STONER et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given above with respect to claim 14.

Independent claim 32 is directed to a packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model. The packet exchange includes a packet memory for storing the entire packet; a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of the multi-port shared memory; and a processor, connected to the layer 2 processing portion and the layer 3 processing portion, for executing a process of a layer higher than layer 3. YOKOYAMA et al., ALBAL et al., and STONER et al. do not disclose or suggest this combination of features.

For example, YOKOYAMA et al., ALBAL et al., and STONER et al. do not disclose or suggest a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of the multi-port shared memory. The Examiner relies on YOKOYAMA et al.'s entry E3 of command descriptor 31 as allegedly corresponding to the recited same memory space and points to col. 9, lines 11 and 18, of YOKOYAMA et al. for support (final Office

Action, pg. 2). Applicants respectfully disagree.

YOKOYAMA et al.'s entry E3 of command descriptor 31 includes a command, a connection identifier (ID), a data length, and a buffer address. YOKOYAMA et al. does not disclose or suggest that these elements of entry E3 of command descriptor 31 are part of a packet. Therefore, YOKOYAMA et al. cannot disclose or suggest a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, as recited in claim 32.

At col. 9, lines 3-20, YOKOYAMA et al. discloses:

> When receiving the CDID from the transport layer (data transfer processor unit 100-1), the data transfer processor unit 100-2 for making the protocol processing of the network layer reads parameters from the second entry E2 of the command descriptor specified by the CDID as shown in FIG. 12 (step 1010), the protocol header is generated in the region specified by the buffer address field F4, in the buffer memory 30 (step 1011), the primitive to the data link layer is generated in the third entry E3 of the command descriptor 31 (step 1012), and then the CDID is supplied through the primitive path 22-3, thereby starting the data transfer processor unit 100-3 of the data link layer (step 1013).
>
> The data transfer processor unit 100-3 of the data link layer first generates the LLC header in accordance with the contents of the third entry E3 of the command descriptor 31 read from the buffer memory as in the network layer (steps 1014 and 1015).

This section of YOKOYAMA et al. discloses generating a primitive to the data link layer in the third entry E3 of command descriptor 31 and that data transfer processor unit 100-3 generates an LLC header in accordance with the contents of the third entry E3. This section of YOKOYAMA et al. does not disclose or suggest a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing

portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, as recited in claim 32.

The disclosures of ALBAL et al. and STONER et al. do not remedy this deficiency in the disclosure of YOKOYAMA et al.

For at least the foregoing reasons, Applicants submit that claim 32 is patentable over YOKOYAMA et al., ALBAL et al., and STONER et al., whether taken alone or in any reasonable combination.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims. Applicants respectfully request that the present amendment be entered since the amendment does not raise new issues or require a further search of the art, but simply improves the form of the claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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